REMARKS/ARGUMENTS

Claims 1-8 and 10-20 are now in the application. Claims 1-8 and 10-12, 14-18 and 20 are amended. Claims 1 and 11 are independent claims.

Support for the Amendments

Support for the claim amendments is found in, for instance, Figures 1 and 2, and the specification on pages 4, line 16 to page 6, line 18.

Claim Objections

The Office Action objects to claims 1, 3-11, 14-15, 18 and 20 for a number of informalities, including:

Reciting, in various claims,

"said blocks" instead of "said functional blocks"

"the steps of" instead of "steps of"

"the internal" instead of "an internal"

"registers" instead of "register element"

"provide control of the selected scan chain to a scan clock signal" instead of "provide a scan clock signal to control the selected scan chain"

"environment" instead of "components".

Applicant has amended the claims as requested by the Examiner and, therefore, requests that this objection be withdrawn and claims 1, 3-11, 14-15, 18 and 20 allowed.

Claim Rejection Under 35 U.S.C. 103(a)

The Office Action rejects claims 1-20 under 35 U.S.C. 103(a) as obvious in view of Baeg (US 5,812,562) and Mehring (US 5,675,729).

Baeg teaches testing an integrated circuit using a test port that has a clock operating at a slower speed than the integrated circuit clock.

The Office Action states that Baeg teaches stopping the clock on the integrated test circuit for testing, but does not teach setting a breakpoint occurring in a functional block on the System On a Chip (SOC).

The Office Action further states that Mehrig teaches performing on-chip measurements using breakpoint signals that cause the stopping of the system clock.

Both Baeg and Mehrig deal with systems that only have one system clock. Neither Baeg nor Mehig teach debugging a system, such as a SOC, that has multiple functional clocks controlling multiple functional blocks.

Applicant's Claim 1 has been amended to recite:

> debugging a system-on-a chip (SoC), the SoC comprising ...least a first and a second functional block, said first function block being controlled by a first block clock and a first clock control unit and said second function block being controlled by a second block clock and a second clock control unit, the method comprising steps of:
>
> setting a first breakpoint on a first specific event occurring on said first functional block;
>
> monitoring events occurring on the SoC;
>
> recognizing occurrence of the first specific event on said first functional block;
>
> providing, responsive to said recognizing, a debug trigger signal to both said first and second clock control units;
>
> halting, responsive to said debug trigger signal, both said first and second block clocks;
>
> determining states of one or more of said system components using a scan clock; and,
>
> utilizing said states to debug the SoC.

SoC's are difficult to debug because each functional unit typically has its own clock. Prior art SoC testing has been limited to the designer needing to halt each functional block separately and, therefore, having no control of the entire SoC device up to the point of failure. Applicant' invention, as embodied in claim 1, enables a designer to set a single break-point in one functional unit of the SoC, and use that break-point to halt all the functional clocks on the SoC and, therefore, all the functional units on the SoC. This allows visibility into the state of the entire SoC at a point of failure, not just the state of the functional unit on which the trigger event occurred.

Baeg and Mehrig, in contrast, are concerned with systems having only one system wide clock. As the Office Action does not show where either Baeg and Mehrig show how to use recognizing an event on one function block to stop the functional clock not only of that

functional block but also at least one other functional clock controlling another function block on the SOC.

The Office Action does not, therefore, show where Baeg and Mehrig anticipate applicant's invention as embodied in claim 1. Applicant requests that this rejection be withdrawn and claim 1 allowed.

Corresponding amendments have been made to independent apparatus claim 11. For the reasons detailed above, the Office Action does not, therefore, show where Baeg and Mehrig anticipate applicant's invention as embodied in claim 11. Applicant requests that this rejection be withdrawn and claim 11 allowed.

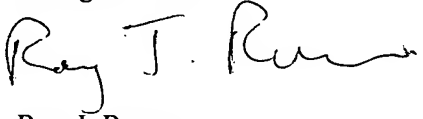
As pending dependent claims 2-8, 10 and 12-20 depend from, and include all the limitations of allowable claims 1 or 11, they too are allowable. Applicant, therefore, requests that the rejection be withdrawn an claims 2-8, 10 and 12-20 be allowed.

Summary

Therefore in view of the foregoing amendments and remarks, applicant respectfully requests entry of the amendments, favorable reconsideration of the application, withdrawal of all rejections and objections and that claims 1-8 and 10-20 be allowed at an early date and the patent allowed to issue.

Respectfully submitted,

Oceager P. Yee

By 

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